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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILSON, SCOTT R	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/982,413	KIANIAN ET AL
	Examiner	Art Unit
	Scott R. Wilson	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,55-65 and 69-74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,55-65 and 69-74* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Election/Restrictions

Applicant's election without traverse of claims 1-28, 55-65 and 69-74 in Paper No. 7 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-11 and 55-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee. As to claim 1, Lee, Figure 2F, discloses an electrically programmable and erasable memory device comprising a substrate (200) of semiconductor material of a first conductivity type, a trench (210) formed into a surface of the substrate, first and second spaced-apart regions (214b) and (214) formed in the substrate and having a second conductivity type, with a channel region therebetween, wherein the second region

(214) is formed underneath the trench, and the channel region includes a first portion (400) that extends substantially along a sidewall of the trench and a second portion (401) that extends substantially along the surface of the substrate, an electrically conductive floating gate (204) disposed over and insulated from at least a portion of the channel region and a portion of the first region, and an electrically conductive control gate (220a) having a first portion (402) disposed in the trench.

As to claim 2, Lee, Figure 2F, discloses that the control gate (220a) has a second portion (403) disposed over and insulated from the floating gate.

As to claim 3, Lee, Figure 2F, discloses that the control gate forms a notch (404) at a connection between the control gate first portion and the control gate second portion.

As to claim 4, Lee, Figure 2F, discloses the floating gate to include a sharp edge that extends toward the notch, at (404).

As to claim 5, Lee, Figure 2F, discloses that the floating gate is disposed over the entire second portion of the channel region (401).

As to claim 6, Lee discloses (col. 4, lines 59-64) that hot electrons penetrate from the control gate to the floating gate, which is within the scope of the floating gate being insulated from the control gate by an insulation layer having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

As to claim 7, Lee, Figure 2F, discloses a layer of insulating material (218b) formed along sidewalls of the trench and extending between the control gate and the floating gate.

As to claim 8, Lee, figure 2F, discloses a first portion of the insulating material (218b) formed along the sidewalls of the trench and between the control gate (220a) and the channel region first portion and a second portion (218a) formed under the control gate (220a) and over the floating gate.

As to claim 9, Lee, Figure 2F, discloses that the channel region first portion extends in a direction directly toward the floating gate.

As to claim 10, Lee, Figure 2F, discloses that the trench has a side wall with an indentation formed therein (405), and wherein the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of the floating gate.

As to claim 11, Lee, Figure 2F, discloses that the trench has a sidewall with an indentation formed therein, the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of the channel region second portion, and that the floating gate is disposed over and insulated from a second part of the channel region second portion.

As to claim 55, Lee, Figure 2F, discloses an electrically programmable and erasable memory device comprising a substrate (200) of semiconductor material of a first conductivity type, a floating gate (204) disposed over and insulated from a surface of the substrate and first and second spaced-apart regions (214b) and (214) formed in the substrate and having a second conductivity type, with a non-linear channel region (400) and (401) therebetween, wherein the channel region defines a path for programming the floating gate with electrons from the second region.

As to claim 56, Lee, Figure 2F, discloses that at least a portion (400) of the non-linearity of the channel region is defined within a plane that is substantially perpendicular to the substrate surface.

As to claim 57, Lee, Figure 2F, discloses that the channel region has a first portion (400) that extends in a direction from the second region (214) directly toward the floating gate (204).

As to claim 58, Lee, Figure 2F, discloses that the direction is substantially perpendicular to the substrate surface.

As to claim 59, Lee, Figure 2F, discloses that the channel region has a second portion (401) that extends in a direction from the channel region first portion (400) to the first region (214b).

As to claim 60, Lee, Figure 2F, discloses that the channel region has a first portion (400) that extends in a direction from the second region (214) toward the surface of the substrate, that the channel region has a second portion (401) that extends in a direction from the channel region first portion (400) to the first region (214b) and that the floating gate (204) is disposed over and insulated from only a portion of the channel region second portion.

As to claim 61, Lee, Figure 2F, discloses an electrically programmable and erasable memory device comprising: a substrate (200) of semiconductor material of a first conductivity type; an electrically conductive control gate (220a) having a first portion (402) formed in the substrate; first and second spaced-apart regions (214b) and (214) formed in the substrate and having a second conductivity type,

with a non-linear channel region (400) and (401) therebetween, wherein the second region (214) is formed underneath and is insulated from the control gate first portion, and the channel region includes a first portion (400) that extends substantially along the control gate first portion (402) and a second portion (401) that extends substantially along a surface of the substrate; and an electrically conductive floating gate (204) disposed over and insulated from at least a portion of the channel region and a portion of the first region.

As to claim 62, Lee, figure 2F, discloses that the control gate has a second portion (403) disposed over and insulated from the floating gate.

As to claim 63, Lee, figure 2F, discloses that the floating gate is disposed over substantially the entire second portion (401) of the channel region.

As to claim 64, Lee, figure 2F, discloses that the channel region first portion (400) extends in a direction directly toward the floating gate (204).

As to claim 65, Lee, Figure 2F, discloses that the floating gate (204) is disposed over only a portion of the channel region second portion.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-28 and 69-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Esquivel et al. in view of Lee. As to claim 12, Esquivel et al., Figure 5, discloses an array of electrically programmable and erasable memory devices comprising a substrate of semiconductor material (56) of a first conductivity type, spaced apart isolation regions (44)(Abstract) formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region (34) and (38)

between each pair of adjacent isolation regions, and a plurality of trenches (54)(Abstract) formed into the surface of the substrate which are substantially parallel to one another and extend across the isolation and active regions in a second direction that is substantially perpendicular to the first direction. Esquivel et al. does not disclose expressly each of the memory cells comprising first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a channel region therebetween, wherein the second region is formed underneath one of the trenches, and wherein the channel region includes a first portion that extends substantially along a sidewall of the one trench and a second portion that extends substantially along the surface of the substrate, and an electrically conductive floating gate disposed over and insulated from at least a portion of the channel region and a portion of the first region, and a plurality of electrically conductive control gates, each extending along one of the active regions, wherein the control gates each have first portions disposed in the trench. Lee, Figure 2F, discloses an electrically programmable and erasable memory device comprising a substrate (200) of semiconductor material of a first conductivity type, a trench (210) formed into a surface of the substrate, first and second spaced-apart regions (214b) and (214) formed in the substrate and having a second conductivity type, with a channel region therebetween, wherein the second region (214) is formed underneath the trench, and the channel region includes a first portion (400) that extends substantially along a sidewall of the trench and a second portion (401) that extends substantially along the surface of the substrate, an electrically conductive floating gate (204) disposed over and insulated from at least a portion of the channel region and a portion of the first region, and an electrically conductive control gate (220a) having a first portion (402) disposed in the trench. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory cell of Lee in the array of Esquivel et al.. The motivation for doing so would have been to form an array of a plurality of cells to store a plurality of bits addressable by bitlines and wordlines. Therefore, it would have been obvious to combine Lee with Esquivel et al. to obtain the invention as specified in claim 12.

As to claim 13, Lee, Figure 2F, discloses that the control gate (220a) has a second portion (403) disposed over and insulated from the floating gate.

As to claim 14, Lee, Figure 2F, discloses that the control gate forms a notch (404) at a connection between the control gate first portion and the control gate second portion.

As to claim 15, Lee, Figure 2F, discloses the floating gate to include a sharp edge that extends toward the notch, at (404).

As to claim 16, Esquivel et al., Figure 5, discloses a layer of isolation material (58) extending along each of the isolation regions and filling portions of the trenches that are in the isolation regions.

As to claim 17, Esquivel et al., Figure 5, discloses the isolation material layer (58) in each of the isolation regions is disposed between a pair of control gates (50) in adjacent active regions. The control gates of Esquivel et al. would be replaced by the control gates of Lee in the combination.

As to claim 18, Lee, Figure 2F, discloses that the floating gate is disposed over the entire second portion of the channel region (401).

As to claim 19, Lee discloses (col. 4, lines 59-64) that hot electrons penetrate from the control gate to the floating gate, which is within the scope of the floating gate being insulated from the control gate by an insulation layer having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

As to claim 20, Lee, Figure 2F, discloses a layer of insulating material (218b) formed along sidewalls of the trench and extending between the control gate and the floating gate.

As to claim 21, Lee, figure 2F, discloses a first portion of the insulating material (218b) formed along the sidewalls of the trench and between the control gate (220a) and the channel region first portion and a second portion (218a) formed under the control gate (220a) and over the floating gate.

As to claims 22 and 23, although not explicitly disclosed, since the first and second regions serve as source and drain, they would necessarily have to be connected electrically to a conductive contact, in order for the memory array to function.

As to claim 24, Lee, Figure 2F, discloses that the channel region first portion extends in a direction directly toward the floating gate.

As to claim 25, Esquivel et al., Figure 5, discloses that the memory cells are formed as pairs of memory cells, wherein each of the memory cell pairs, i.e. adjacent floating gates (34), share a single

second region (38) therebetween, which would be embodied in the combination by the second region of Lee (214).

As to claim 26, Lee, Figure 2F, discloses that the trench has a side wall with an indentation formed therein (405), and wherein the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of the floating gate.

As to claim 27, Lee, Figure 2F, discloses that the trench has a sidewall with an indentation formed therein, the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of the channel region second portion, and that the floating gate is disposed over and insulated from a second part of the channel region second portion.

As to claim 28, Esquivel et al., Figure 5, discloses that the second regions, which would be embodied in the combination by the second regions of Lee (214) would be integrally formed together in one of a plurality of conductive lines buried in the substrate, and wherein each of the conductive lines would extend in the second direction and include a raised portion that would extend up to the substrate surface.

As to claim 69, Esquivel et al., Figure 5, discloses an array of electrically programmable and erasable memory devices comprising a substrate of semiconductor material (56) of a first conductivity type and having a surface, spaced apart isolation regions (44)(Abstract) formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region (34) and (38) between each pair of adjacent isolation regions, where each of the active regions includes a plurality of memory cells and wherein each of the memory cells includes an electrically conductive floating gate (34) disposed over and insulated from the substrate surface. Esquivel et al. does not disclose expressly a plurality of first regions formed in the substrate and having a second conductivity type, each of the first regions extends across the active regions in a second direction perpendicular to the first direction and is disposed at least partially underneath one of the floating gates in each of the active regions or a plurality of second regions formed in the substrate and having the second conductivity type, each of the second regions extends across the active regions in the second direction and is disposed between a pair of the first regions, wherein the second regions are buried underneath the substrate surface; and a plurality of

electrically conductive control gates each extending along one of the active regions in the first direction. Lee, Figure 2F, discloses what would be embodied in the combination as a plurality of first regions (214b) formed in the substrate and having a second conductivity type, each of which would extend across the active regions in a second direction perpendicular to the first direction and would be disposed at least partially underneath one of the floating gates (204), which would replace floating gates (34) of Esquivel et al., in each of the active regions, and what would be embodied in the combination as a plurality of second regions (214) formed in the substrate and having the second conductivity type, each of the second regions extending across the active regions in the second direction and disposed between a pair of the first regions, wherein the second regions are buried underneath the substrate surface, and finally, what would be embodied in the combination as a plurality of electrically conductive control gates (220a) each extending along one of the active regions in the first direction. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the memory cell of Lee in the array of Esquivel et al.. The motivation for doing so would have been to form an array of a plurality of cells to store a plurality of bits addressable by bitlines and wordlines. Therefore, it would have been obvious to combine Lee with Esquivel et al. to obtain the invention as specified in claim 69.

As to claim 70, Lee, Figure 2F, discloses each of the control gates would include a plurality of first portions (402) that are each disposed in the substrate and over one of the second regions.

As to claim 71, Lee, Figure 2F, discloses that the control gate therein would have a second portion (403) that is disposed over and insulated from the floating gates (204).

As to claim 72, Lee, Figure 2F, discloses what would be embodied in the combination as a plurality of channel regions (400) and (401) in the substrate each extending between one of the first regions and one of the second regions.

As to claim 73, Lee, Figure 2F, discloses that each of the channel regions would have a first portion (400) extending from one of the second regions toward the substrate surface, and a second portion (401) extending substantially along the substrate surface.

As to claim 74, Lee, Figure 2F, discloses that the second regions would be integrally formed

together in one of a plurality of conductive lines buried in the substrate, wherein each of the conductive lines would extend in the second direction and would include a raised portion that extends up to the substrate surface.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

srw
July 25, 2003

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